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10/532,889	04/27/2005	Katsuhiko Morosawa	05246/LH	2247

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/532,889	MOROSAWA ET AL.	
	Examiner	Art Unit	
	SHAHEDA A. ABDIN	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 June 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-78* is/are pending in the application.

4a) Of the above claim(s) *8, 19, 30-34, 38-63 and 73-78* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,9-18,20-29,35-37 and 64-73* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 June 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's election without traverse of species E of Figs. 10-29, and claims 1-7, 9-18, 20-29, 35-37, and 64-73 reads on the species E, in the reply filed on 05/26/2009 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-5, 9,12-13,16-18,20-23,26-27, and 35-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kasai (US Pub. No: 20030040149A1).

(1) Regarding claim 1:

Kasai teaches in a display device (in Fig. 2 and 5) for displaying image information (i.e image at display pixel) according to a display signal (i.e. signal atX1-Xm) consisting of digital signals (data corresponding to a bit, [0048]) comprising: a display panel (i.e. 101) comprising a plurality of signal lines (i.e. X1-Xm) and a plurality

of scanning lines (i.e. Y1-YN) which intersect at right angles with each other, and a plurality of display pixels (plurality of display pixels 200) with optical elements (i.e. EL element) arranged near the intersecting point of the plurality of signal lines and the plurality of scanning lines ([0029-0030]),

a scanning driver circuit (i.e. 103) for sequentially applying a scanning signal to each of the scanning lines for setting the selective state (position) of each line of each display pixel ([0029], [0031]- [0034]) ; and

a signal driver circuit (i.e. 102) comprising a plurality of current generation circuits (300, Fig. 2) [0034]); the current generation circuits (300) comprise at least a gradation current generation circuit (310) and a drive current generation circuit (320) [0008-0009] [0048]; the gradation current generation circuit (310) generates a plurality of gradation currents (note that 310 corresponding to IU1-IU8 generates a gradation current Iout) corresponding to each of the display signal bits (i.e.8 bit data or 25 pixel level) based on constant , predetermined reference current [0009], and the drive current generation circuit (320) generates drive current from the plurality of gradation currents (current from 310) based on the value of the display signal which supplies the generated drive current to each signal line (data lines) ([0043-0044], [0053] , [0061], and Fig. 5).

(2) Regarding claim 2:

Kasai teaches each current generation circuit (i.e. 300) sets the signal polarity (i.e. control electrode signal) of the drive current (i.e. I. Sub. m, [0072]) so that the drive current flows in the direction drawn from the display pixels side (i.e. pixel circuit 200) [0055], [0075].

(3) Regarding claim 3:

Kasai teaches each current generation circuit (i.e. 300) sets the signal polarity of the drive current so the drive current (i.e. I. Sub. m, [0072) flows in the direction poured into the display pixels [200].

(4) Regarding claim 4:

Kasaki teaches each of a plurality of current generation circuits (i.e. 300) in the signal driver circuit is provided corresponding to each of a plurality of the display pixels (i.e. 200) of each scanning line (Y1-YN) of the display panel (101) (Fig. 2, [0031]).

(5) Regarding claim 5:

Kasaki teaches each current generation circuit (300) supplies the drive current simultaneously corresponding to each of a plurality of pixels of each scanning line (gate line 304, 303, Fig. 5) ([0049]).

(6) Regarding claim 9:

Kasai teaches wherein the drive current generation circuit (300) comprises a switching circuit (e.g. 81-88, Fig. 5) for selecting the gradation current from the plurality of gradation currents in response to each bit value (each data bit for the display pixel) of the display signal [0048-0049].

(12) Regarding claim 12:

Kasai teaches wherein the current value (Iout) of the plurality of gradation currents have a different ratio with each other specified by 2n (n=0, 1, 2 and 3, . . .) ([0049-0052]).

(7) Regarding claim 13:

Kasai teaches wherein each gradation current generation circuit (310) comprises a plurality of gradation current transistors (e.g. 81-88, Fig. 5) for generating a plurality of gradation currents [0048-0049].

(8) Regarding claim 16:

Kasai teaches wherein each gradation current generation circuit (310) comprises a reference voltage generation circuit (400) for generating reference voltage based on the reference current (I const) ([0058]).

(9) Regarding claim 17:

Kasai teaches wherein the reference voltage (400) generation circuit comprises reference current transistors (e.g. 71 and 72 corresponding to 51 and 31) for generating reference voltage to the control terminals (0059); the reference current is supplied to the current path (304); the reference current transistor control terminals are connected in common to the control terminals of the plurality of gradation current transistors (81-88) ([0058-0060].

(10) Regarding claim 18:

Kasai teaches wherein the reference current transistors (71 and 72 corresponding to 51 and 31) and the plurality of gradation current transistors (81-88) constitute a current mirror circuit (see the abstract).

(12) Regarding claim 20:

Kasai teaches, wherein each gradation current generation circuit (310) further comprises a reference voltage generation circuit (400) for generating reference voltage based on the reference current (Iconst) ([0058], and Fig. 5).

(13) Regarding claim 21:

Kasai teaches wherein the reference voltage generation circuit (400) comprises an electric charge storage circuit (capacitor 230 which is corresponding to pixel associated with the reference voltage generation circuit 400, see Fig. 3 and 5) for storing the electric charge in response to the current component of the

reference current (Iconst) ([0036]) .

(14) Regarding claim 22:

Kasai teaches the signal driver circuit (data driving circuit 102) comprises:

a reference current supply line (402 corresponding to 304, Fig. 5) for supplying the reference current (Iconst); and,

a structure in which the reference current (Iconst) is supplied to the plurality of gradation current generation circuits (i.e. 310 for each pixel) via the reference current supply line (402 corresponding to 304) ([0053], and [0058]).

(15) Regarding claim 23:

Kasai teaches wherein each gradation generation circuit (300) comprises a supply control switching circuit (520, see Fig. 8) for controlling the supply state (position) of the reference current (Iconst) from the reference current supply line (402 corresponding to 304) to the proper gradation current generation circuit (310); the supply control switching circuit selectively performs switching control so the reference current may be supplied only to any one gradation current circuit of the plurality of gradation current generation circuits ([0074-0076]).

(16) Regarding claim 26:

Kasai teaches that each current generation circuit (i.e. 300) further comprises a specified state setting circuit (i.e. i.e. shift register 500) for

setting the signal lines to a specified voltage which makes the optical elements (EL elements of the pixel 200) drive in a specified operating state (i.e. on state or off state of the switches) when the display signal has a specified value (i.e. specific level of the pixel) ([0074]).

(17) Regarding claim 27:

Kasai teaches wherein the drive current is generated for selecting the gradation currents according to each of the display signal bits ([0048-0049]); the display signal specified value is a value (e.g. 8 bit) from which all of each of the gradation currents (e.g. IU1-IU2) is non-selected (non selected in when switching transistor is in off state) from the display signals ; the specified voltage (i.e. voltage in off state) is the voltage for setting the optical elements drive in a state of lowest gradation (0060-0061).

(18) Regarding claim 35:

Kasai teaches wherein the optical elements in the display pixels (200) comprise light emitting elements (OEL) for accomplishing light generation operation by way of luminosity gradation according to the current value (Iout) of the supply current ([0002], and [0047-0049], Fig. 5).

(19) Regarding claim 36:

Kasai teaches the light emitting elements comprise organic electroluminescent elements (OEL 220) ([0047]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 6-7, 10-11, 24-25,28-29, 37 and 64-73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai US Pub No. 2003/0040149 in view of Yamazaki (US Patent No: 6528951 B2).

(1) Regarding claim 6:

Note that Kasai teaches each current generation circuit (300) but Kasaki does not disclose current generation circuit comprises a signal holding circuit which takes in and holds the display signal.

However, Yamazaki in the same field of endeavor discloses current generation circuit (8801) comprises a signal holding circuit (8802) which takes in and holds the display signal (column 25, lines 5-28) .

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of signal holding circuit as taught by Yamazaki in to the current generation circuit of Kasai so that the current generation circuit could be comprised a

signal holding circuit which takes in and holds the display signal. In this configuration the system would provide a improved quality image in the EL display device (column 5, lines 9-12).

(2) Regarding claim 7:

Yamazaki teaches wherein the drive current generation circuit (8801) generates the drive current (current through S_a to S_d) based on the value of the display signal held in the signal holding circuit (8802) (column 25, lines 5-28) .

(3) Regarding claim 10:

Yamazaki teaches the current generation circuit (880) further comprises a signal holding circuit (8802) for taking in and holding the display signal (i.e. display data) (column 25, lines 5-28) .

(4) Regarding claim 11:

Note that Yamazaki teaches wherein the signal holding circuit (8802) comprises a plurality of latch circuits (S_LAT, S_LATb) which take in and hold each bit of the display signal and output an output signal responsive to each bit (i.e. each pixel value) (column 25, lines 5-28) and Kasai teaches the switching circuit (81-88) selects the

gradation currents. Therefore, combining the reference of Kasai and Yamazaki would have been obvious to generate the current drive based on the output of the plurality of latch circuits.

(5) Regarding claim 24:

Yamazaki teaches each current generation circuit (8801) comprises a signal holding circuit (8802) for taking in and holding (latching) the display signal (column 25, lines 5-28).

(6) Regarding claim 25:

Note that Yamazaki teaches, supply control switching circuit (switches in Fig. 15 and 16) timing of the switching control synchronizes (i.e. sampling) with the timing of the signal holding circuit at the time of taking in and holding the display signal (display data signal) (column 25, lines 5-47).

Therefore, it would have been obvious to a person of ordinary skill in the art t incorporate the method of the supply control switching circuit timing of the switching control synchronizes with the timing as taught by Yamazaki in to the supply control switching circuit of Kasai so that the supply control switching circuit could be timing of the switching control which synchronizes with the timing of the signal holding circuit at the time of taking in and holding the display signal.

(7) Regarding claim 28:

Note that Kasai teaches the specified state setting circuit (shift register 500) but Kasai does not teach that the state setting circuit (i.e. shift register) comprises a specified digital value judgment section (i.e. logic circuit) for judging whether or not the display signal is the specified value, and a specified voltage application section for applying the specified voltage to the signal lines based on the judgment result by the specified digital value judgment section.

However, Yamazaki in the same field of endeavor teaches the state setting circuit (i.e. shift register 8801) comprises a specified digital value judgment section (logic circuit) for judging whether or not the display signal (display data) is the specified value (e.g. 0 or 1 logic), and a specified voltage application section (voltage terminal) for applying the specified voltage to the signal lines (line for the transistor) based on the judgment result by the specified digital value judgment section (i.e. logic section) (see the illustration of Fig. 21, 22, and column 26, lines 5-40).

Therefore, combining the reference of Kasai and Yamazaki would be obvious to one of ordinary skill in the art to have the limitations that is "the state setting circuit (i.e. shift register) could be comprised a specified digital value judgment section for judging whether or not the display signal is the specified value, and a specified voltage application section for applying the specified voltage to the signal lines based on the judgment result by the specified digital value judgment section". In this configuration

the system would provide a improved quality image in the EL display device (column 5, lines 9-12).

(8) Regarding claim 29:

Yamazaki teaches, wherein the specified digital value judgment section (logic circuit in Fig. 21) performs judgment of whether or not said display signal is the specified value based on the logical sum of each bit value (i.e. the values from the logic circuit) of the digital signals of the display signals (display data) (column 5, lines 9-12).

(9) Regarding claim 37:

Note that Yamazaki teaches wherein the display pixels (104) comprise at least a pixel driver circuit (i.e. 102, 103, Fig. 4); the pixel driver circuit includes a voltage holding circuit (e.g. latches 8802, 8803) for holding the voltage component (voltage signals) in response to the drive current supplied from the signal driver circuit (e.g. source sisignal driver 102, Fig. 4); and a current supply circuit (i.e. transistors in Fig. 21) for supplying luminescent drive current to the light emitting elements (OEL 220) based on the voltage component held in the voltage holding circuit and for making the light emitting elements emit light (column 25, lines 15-28 and column 26, lines 30).

(10) Regarding claim 64:

Kasai teaches a method for driving the display device which displays image information (image at pixel) according to display signals (source signal) consisting of digital signals (data corresponding to a bit, [0048]) in a display panel (101) comprising a plurality of display pixels (200) provided with optical elements (i.e. EL elements) arranged close to the intersecting point of a plurality of signal lines and a plurality of scanning lines (Yi-YN) ([0029-0030]), the method comprising:

each of the display signal bits (data bit) based on constant, predetermined reference current [constatant current Iconst]; and supplying the drive current to the plurality of signal lines (i.e. plurality of source signal lines X1-XM) ([0029], [0031]-[0034]), , a plurality of gradation currents generated (i.e. generated at 310) ([0008-0009], and [0048]) corresponding to each of the display signal bits (display data bit) based on constant, predetermined reference current [constant current Iconst]; and supplying the drive current to the plurality of signal lines (i.e. plurality of source signal X1-XM) ([column 12, lines 25-30]),

Note that Kasai does not disclose taking in and holding (holding at the latch) the display signal corresponding to the plurality of display pixels ; and generating drive current according to a value of the held display signal.

Yamazaki in the same field of endeavor discloses taking in and holding (holding at 8802) the display signal corresponding to the plurality of display pixels (column 13,

lines 45-52) ; and generating drive current according to a value of the held display signal (signal at 8802).

Therefore, it would have been obvious to a person of ordinary skill in the art to incorporate the method of signal holding circuit as taught by Yamazaki in to the current generation circuit of Kasai so that taking in and holding (holding at 8802) the display signal could be corresponding to the plurality of display pixels; and drive current could be generated according to a value of the held display signal. In this configuration the system would provide a improved quality image in the EL display device (column 5, lines 9-12).

(11) Regarding claim 65:

Kasai teaches a current value of the plurality of gradation currents have a different ratio with each other specified by 2n (n=0, 1, 2 and 3, . . .) (0050-0051).

(12) Regarding claim 66:

Kasai teaches the generating drive current step includes selecting (determining) and integrating (combine together) corresponding to the gradation currents (e.g. IU1-IU2)) in response to each bit value of the display signal (0059-0060).

(13) Regarding claim 67:

Kasai teaches the signal polarity (polarity set by the transistor for the pixel 200, see Fig. 3) of the drive current is set so the drive current flows in the direction drawn from the display pixels ([0036], and [0090]).

(14) Regarding claim 68:

Kasai teaches the signal polarity (polarity set by the transistor of the pixel) of the drive current is set so the drive current flows in the direction pour into the display pixels ([0036], and [0090]).

(15) Regarding claim 69:

Kasai teaches the optical elements (EL elements) in the display pixels (200) comprise light emitting elements (220) which accomplish light generation operation by way of luminosity gradation according to the current value of the supply current ([0047]).

(16) Regarding claim 70:

Kasai teaches wherein the light emitting elements comprise organic electroluminescent elements (i.e. 220, Fig. 2) ([0047]).

(17) Regarding claim 71:

Yamazaki teaches,: holding the voltage component (holding the voltage component at 8802) corresponding to the drive current (display data drive current);

supplying luminescent drive current to the light emitting elements (i.e. EL) based on the voltage component held in the voltage holding circuit (I.E. Latch circuit), which makes the light emitting elements emit light (column 25, lines 15-28 and column 26, lines 30).

(18) Regarding claim 72:

Yamazaki teaches judging (judging at logic circuit) whether or not the display signal is a specified value (specific value for the pixel circuit);
applying the specified voltage which makes the display pixels drive in a specified operating state (on or Off state) to the signal lines (i.e. display signal lines I) when judged the display signal as being the specified value ((column 13, lines 45-52)).

(19) Regarding claim 73:

Kasai teaches wherein the drive current is generated for selecting the gradation currents according to each of the display signal bits ([0048-0049]); the display signal specified value is a value (e.g. 8 bit) from which all of each of the gradation currents (e.g. IU1-IU2) is non-selected (non selected in when switching transistor is in off state) from the display signals ; the specified voltage (i.e. voltage in off state) is the voltage for setting the optical elements drive in a state of lowest gradation

6. Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai.

(1) Regarding claim 14;

Note that Kasai teaches wherein the plurality of gradation current transistors (e.g. 81-88) and each control terminal (control terminal for each transistor) connected in parallel; the gradation currents flow in the current path of each of the gradation current transistors (see the illustration in Fig. 5, see the abstract, and [0048-0049]), but Kasai does not specifically discloses that "**each transistor differs in size** ". However, such limitations are merely a matter of obvious choice and would have been obvious in the system of "Kasai". The limitations do not define a patentably distinct invention over that in "Kasai" since the invention as a whole and "Kasai" are directed to plurality of gradation current transistor (i.e. 81-88) and which is connected in parallel to each other.

Therefore, to have the limitations "**each transistor differs in size**", "Kasai" would have been a matter of obvious choice to one of ordinary skill in the art, since it has been held that discovering an optimum value (i.e. size) of a result effective variable involves only routine skill in the art. In re Boesch, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

(2) Regarding claim 15:

Kasai teaches, wherein the channel width of each gradation current transistor is set at a different ratio with each other specified by 2n (n=0, 1, 2 and 3, . . .) ([0050-0051]).

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's discloser.

Okuyama (US Patent No: 6556176 B1) discloses an active type EL display device capable of displaying digital video signal.

Inquiry

8. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Shaheda Abdin whose telephone number is (571) 270-1673.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard HJerpe could be reached at (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pari-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO

Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Shaheda Abdin

07/16/2009

/Regina Liang/

Primary Examiner, Art Unit 2629